REMARKS

Applicants respectfully request reconsideration of the present U.S. Patent application as amended herein. Claims 2, 3, 7, 8 and 11 have been amended. No claims have been added or canceled. Thus, claims 1-16 are pending.

Objection to the Abstract

The abstract as originally filed was objected to for including phrases that could be implied, such as "the invention" appearing in line 2 of the abstract. A substitute abstract is included herewith. Applicants request that the original abstract be replaced with the substitute abstract. Applicants submit that the substitute abstract overcomes the objections set forth in the Office Action. Therefore, Applicants request that the objection to the abstract be withdrawn.

Objection to the Drawings

The drawings were objected to because block element "856" as shown in Figure 8 of the drawings is not identified in the specification. A brief description of block element 856 has been added to the specification by this amendment. No new matter has been added. Therefore, Applicants request that the objection to the drawings be withdrawn.

Objection to the Claims

Claims 2, 3, 7 and 8 were objected to for informalities. Claims 2, 3, 7 and 8 have been amended as suggested in the Office Action. Therefore, Applicants request that the objections to claims 2, 3, 7 and 8 be withdrawn.

Claim Rejections - 35 U.S.C. § 112

Claims 11-16 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Specifically, in claim 11, line 6, "the texture palette" has no clear antecedent basis. Claim 11 has been amended to provide proper antecedent basis. Therefore, Applicants request that the rejection of claim 11-16 under 35 U.S.C. § 112, second paragraph be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Claims 11-13 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,892,518 issued to Mizobata, et al. (*Mizobata*). For at least the reasons set forth below, Applicants submit that claims 11-13 are not anticipated by *Mizobata*.

Claim 11 recites:

> a memory coupled to the command stream controller and to the write address generator, ***the memory to store pixel data in a first order determined by the write address generator***;
>
> processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and
>
> a read address generator coupled to the processing circuitry and to the memory, ***the read address generator to cause the memory to output pixel data in a second order***.

Thus, Applicants claim storing data to memory in a first order and reading the data from the memory in a second order. For example, the specification describes one embodiment of the ordering as:

> ***Write address generator 640 causes correction data for the pixels of a macroblock to be written to texture palette 650 block by block in row major***

> ***order***. In other words, the first row of block 710 (pixels 0-7) is written to texture palette 650 followed by the second row of block 710 (pixels 16-23). The remaining rows of block 710 are written to texture palette 650 in a similar manner.
>
> ...
>
> Read address generator 660 causes pixel information to be read from texture palette 650 in an order different than written as controlled by write address generator 640. Referring to Figure 7, ***read address generator 660 causes pixel data to be read from texture palette 650 sub-block-by-sub-block in row major order***. This ordering optimizes performance of cache 630 due to locality of reference of pixels stored therein. In other words, the first row of sub-block 712 (pixels 0-3) are read followed by the second row of sub-block 712 (pixels 16-19). The remaining pixels of sub-block 712 are read in a similar manner.

See page 11, lines 17-21 and page 15, line 19 to page 16, line 3.

Mizobata discloses that image data are written to memory and read from memory. See, for example, col. 30, lines 25-32. However, *Mizobata* does not disclose the order in which data is either written to or read from memory. Therefore, *Mizobata* does not anticipate the invention as claimed in claim 11.

Claims 12 and 13 depend from claim 11. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 12 and 13 are not anticipated by *Mizobata* for at least the reasons set forth above.

Claim Rejections - 35 U.S.C. § 103

Claims 1-10 and 14-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Mizobata* in view of U.S. Patent No. 5,748,789 issued to Lee, et al. (*Lee*). For at least the reasons set forth below, Applicants submit that claims 1-10 and 14-16 are not rendered obvious by *Mizobata* and *Lee*.

Claim 1 recites the following:

> ***storing the correction data in a memory according to a first order*** corresponding to the motion compensation command;

performing frame prediction operations in response to the motion compensation command;

reading the correction data from the memory according to a second order...

Thus, Applicants claim storing data to memory in a first order and reading the data from the memory in a second order. Claim 6 recites similar limitations.

As discussed above, *Mizobata* does not teach or suggest storing data to memory in a first order and reading the data from the memory in a second order. *Lee* is cited to teach transparent block skipping in object-based video coding systems including use of a bounding box, texture operations, etc. Whether or not *Lee* teaches the elements set forth in the Office Action, *Lee* does not cure the deficiencies of *Mizobata*. Therefore, no combination of *Mizobata* and *Lee* teaches or suggests the invention as claimed in claims 1 and 6.

Claims 2-5 depend from claim 1. Claims 7-10 depend from claim 6. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 2-5 and 7-10 are not rendered obvious by *Mizobata* and *Lee* for at least the reasons set forth above.

Claims 14-16 depend from claim 11, which was discussed above. Applicants submit that claims 14-16 are similarly not rendered obvious by *Mizobata* and *Lee*.

Conclusion

For at least the foregoing reasons, Applicants submit that the objections and rejections have been overcome. Therefore, claims 1-16 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully

requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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ANNOTATED CHANGES TO THE SPECIFICATION AND CLAIMS

IN THE SPECIFICATION

Page 7, lines 13 to 16:

> **Figure 2** is a block diagram of an MPEG-2 decoding process suitable ffor use with the invention. Coded [decoded] video data 200 is obtained. Coded [decoded] video data 200 can come from either a local (e.g., memory, DVD, CD-ROM) or remote (e.g., Web server, video conferencing system) source.

Page 18, lines 9 to 15:

> In the example of Figure 8, motion compensation circuitry 840 reconstructs B frame 858 from I frame 852 and P frame 854. In one embodiment, the various frames are stored in video memory 850. B frame 856 can also be stored in video memory 850. Alternatively, the frames can be stored in memory 830 or in some other memory. If, for example, motion compensation circuitry 840 were rendering a B frame a single frame would be read from video memory 850 for reconstruction purposes. In the example of Figure 8, four frames are stored in video memory 850; however, any number of frames can be stored in video memory 850.

IN THE CLAIMS

2. (Amended) The method of claim 1 wherein the first order is based on output from an Inverse Discrete Cosine Transformation (IDCT) operation.

3. (Amended) The method of claim 1 wherein performing frame prediction operations further comprises:

generating a bounding box containing the macroblock;

iterating the bounding box;

fetching reference pixels;

filtering the reference pixels;

averaging the filtered reference pixels, if necessary; and

adding correction data to the reference pixels.

7. (Amended) The apparatus of claim 6 wherein the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation.

8. (Amended) The apparatus of claim 6 wherein performing frame prediction operations further comprises:

means for generating a bounding box containing the macroblock;

means for iterating the bounding box;

means for fetching reference pixels;

means for filtering the reference pixels;

means for averaging the filtered reference pixels, if necessary; and

means for adding correction data to the reference pixels.

11. (Amended) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory [texture palette] to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in a second order.